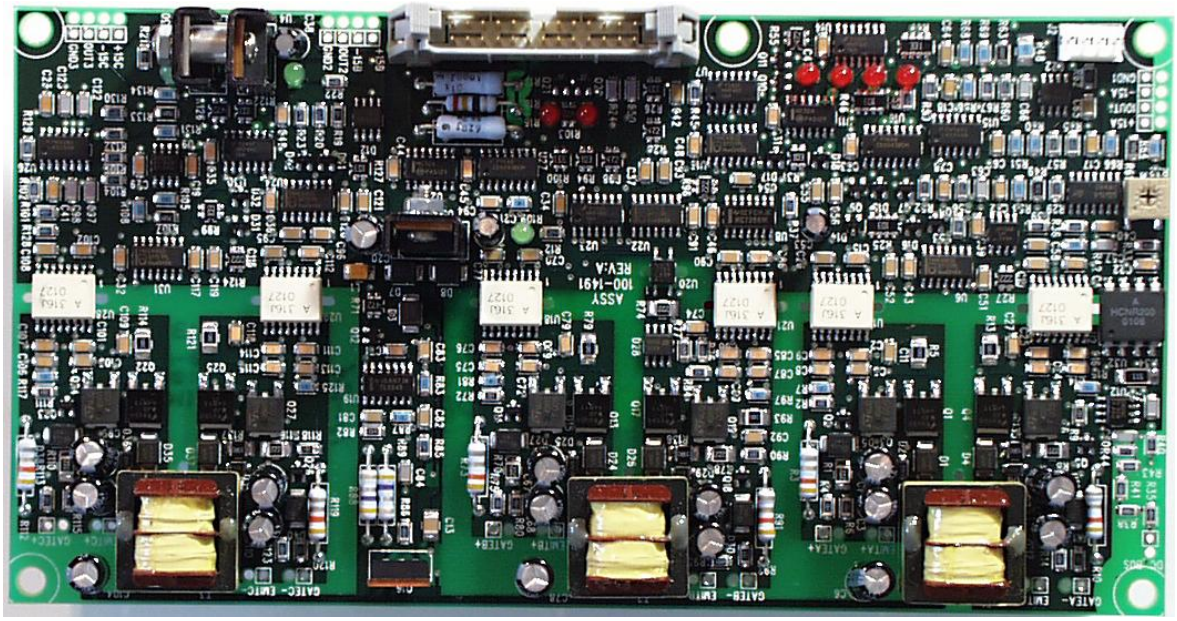
BAP1491 IGBT Gate Drive Board for Three Phase and Full Bridge Inverters



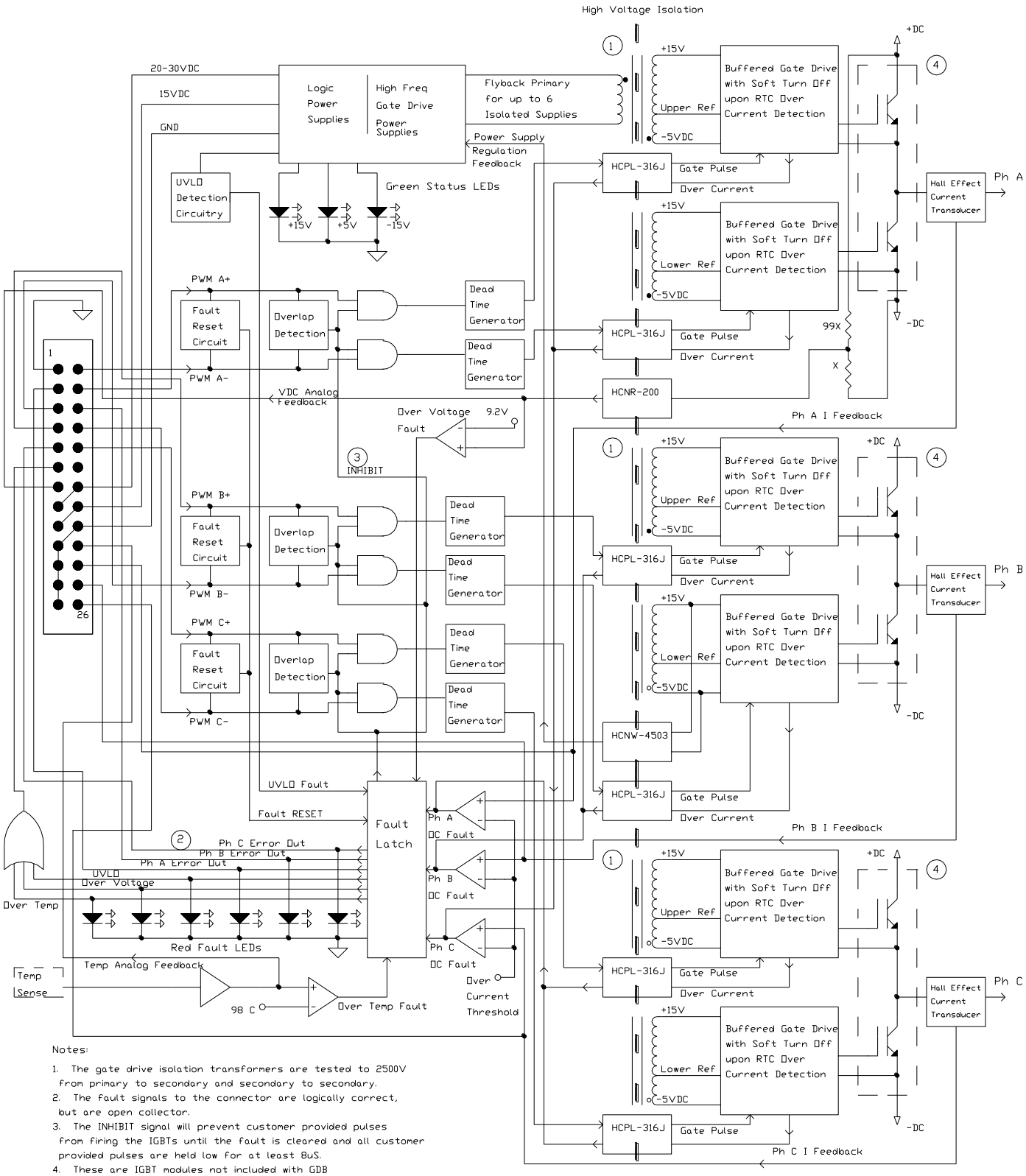
Complete IGBT Gate Drive Board with the following feature:

- Current sensing and heatsink temperature sensing capability
- Over voltage protection
- Includes all power supplies
- DC link voltage sensing
- Over current protection
- Single 26 pin header for all I/O and input power
- Under voltage lock-out
- Diagnostic LEDs
- Automatic dead time generation
- Shoot through protection

Introduction

The BAP1491 Insulated Gate Bipolar Transistor (IGBT) Gate Drive Board (GDB) discussed in this Datasheet/Application Note provides a safe, reliable, isolated interface between control logic and an IGBT based power stage. With minimal development time and cost, an effective inverter can be designed and built using the techniques described below.

Typically, the most unreliable portion of an inverter design is the power stage. In most if not all cases, this is due to inadequate control of the power semiconductors. The APS IGBT GDB is a robust design (see **Figure 1** Block diagram) offering the necessary protection features to ensure a reliable power stage including: two forms of over current protection, DC link over voltage protection, over temperature protection, and under voltage lockout. Also provided as feedback signals to the control logic are isolated, analog, real-time representations of each phase output current, the DC link voltage and a temperature sensor interface that can be mounted on a heatsink.



Notes:

1. The gate drive isolation transformers are tested to 2500V from primary to secondary and secondary to secondary.
2. The fault signals to the connector are logically correct, but are open collector.
3. The INHIBIT signal will prevent customer provided pulses from firing the IGBTs until the fault is cleared and all customer provided pulses are held low for at least 8uS.
4. These are IGBT modules not included with GDB

Circuit Description

GDB Power Supply

The BAP1491 Gate Drive Board requires either an unregulated 24 (20-30) volt or regulated 15 (14.5-15.5) volt power supply to operate (see **Table 1** for pin assignments). The system designer must choose one supply or the other, whichever is available or preferred. **Note:** Connecting both power supplies simultaneously will create contention issues that may result in damage to the board.

The input voltage is used to generate the logic control power supplies and the required isolated bipolar power supplies for each individual IGBT. The power consumed by the 24-volt or 15-volt supply is proportional to the gate charge and the switching frequency of the IGBT being driven. The larger the IGBT in a particular manufacturer's series, the larger the gate charge, therefore the more power it will consume.

The graph in **Figure 2** depicts the estimated power consumption vs. switching frequency for a three-phase bridge configuration employing three dual IGBTs, each with a gate charge of 1100ηC. The value at zero Hz is the power consumed by the GDB before switching IGBTs of any current rating. The power consumed increases with switching frequency and is proportional to the gate charge. To determine the power required for a specific application, look up the gate charge (usually given in ηC on the data sheets) of the selected IGBT and offset the power consumed by the GDB at zero Hz by the power consumed by switching IGBTs.

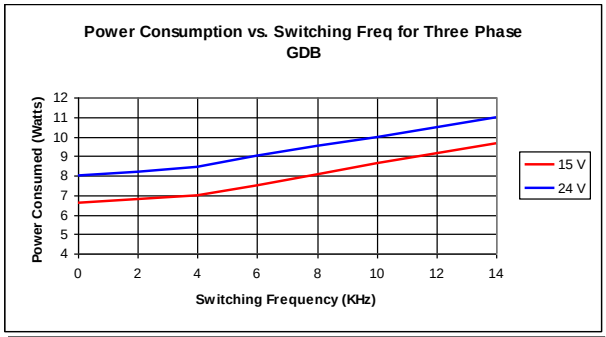


Figure 2: GDB Power Consumption vs. switching frequency.

Note: It is not recommended to run a standard three-phase bridge, with IGBTs having a gate charge of 1500ηC, beyond 20KHz. Excessive heating of gate drive transistors may occur, resulting in potential damage to the board. Factory modifications are available to the standard board for operation up to 30KHz under the above stated conditions. **Figure 8** depicts the maximum recommended frequency vs. gate charge.

Control Signals

The customer provided control signals that determine the IGBT conduction state require 0 volts for an OFF command and 15 volts for an ON command. The GDB can be modified to accept TTL level PWM control signals. Please refer to the FAX form at the end of this Datasheet/Application Note. These signals are referenced to the GDB power supply ground. For three-phase inverter applications, these signals are inputs into pins PWMA+, PWMA-, PWMB+, PWMB-, PWMC+ and PWMC- on connector J1 (pin assignments located in **Table 1**). These signals are fed through Schmitt-triggered buffers to ensure fast edges for overlap detection and dead time generation circuitry.

The overlap detection circuitry inhibits a complimentary pair of IGBTs (i.e. IGBTA+ and IGBTA- in **Figure 3**) from firing simultaneously, which would result in a potentially destructive shoot through current. If an overlap is detected, both the upper and lower IGBTs are held off until one of the IGBT control inputs (PWMX+ or PWMX-) go low, at which point the IGBT still commanded high will turn on.

Dead time, which is a delay from when the customer provided control signal goes high to when the on signal is applied to the gate of the IGBT, is generated on board. Therefore, dead time is neither required nor desired on the control signals. Customer provided dead time may effect the RESET function described in the Protection Features section below. Standard dead time is set to approximately 2μs, consult factory for alternate dead time settings (see APS Fax Request Form attached to the end of this Application Note).

Gate Drive Signals

After the control signals are integrated with dead time, they are optically isolated and buffered by a transistor stage with the capability to source the high peak currents necessary to turn large IGBTs on and off quickly. The GDB is equipped with 4.3-Ohm gate resistors standard that allow up to a 3 Amp peak current pulse. This resistor is selected to optimize the performance of an IGBT with a gate charge of approximately 1000ηC; however, it will work in many applications. Consult factory for alternate gate resistor values.

The isolated gate drive power supplies are generated with three separate high frequency transformers. These transformers are high potential tested to 2500 volts between each of its three windings. The primary of each transformer is referenced to the ground of the 24-volt or 15-volt power supply.

Each secondary is referenced to an emitter of an IGBT in a phase. The capacitance between the secondaries is less than 15pF to minimize capacitive coupling between upper and lower IGBTs.

Each secondary creates a bipolar power supply that is optimally regulated to sufficiently drive the IGBT into saturation, yet low enough to limit short circuit currents and minimize power supply consumption. A negative bias is provided when the IGBT is off to ensure it remains off and to minimize turn off losses.

Current Sensing

The APS GDB is specifically designed to operate with open loop Hall effect sensors. The GDB provides the necessary ±15-volt power supplies and ground reference for three separate current sensors (see **Figure 4**). An isolated voltage proportional to output current is fed back to the GDB where it is buffered and fed back to the customer provided controller (see **Table 1** for pin assignments) as a real time analog representation of the output currents.

The gain of the signal conditioning circuitry on the GDB is set to unity. Therefore, if the Hall effect sensor's output is 4 volts, the voltage fed back to the customer provided controller would be 4 volts. The scaling of the output current feedback, along with the over current threshold can be adjusted to a specific application. The default scaling is illustrated in **Figure 9**. **Note:** The Hall effect sensors must be mounted with its current direction arrow facing in towards the IGBT.

DC Link Voltage Sensing

The positive of the DC link should be fed back to the GDB for monitoring and protection (see **Figure 3**). The reference for the DC link sense wire is the emitter of the lower IGBT of phase A (EMIT A-), which is also the ground of the DC link. This voltage is attenuated by a voltage divider (100:1) and transmitted across an optical barrier to provide an isolated, logic level representation of the DC link now referenced to the ground of the GDB power supply. The attenuated voltage is available on pin 13 of J1 (600 volts on the DC link will result in 6.0 volts at pin 13) and is also used by the control logic to detect an over voltage condition (default threshold of 910 ±10 VDC).

Temperature Sensing

The GDB temperature sense circuit uses an LM35, a low cost, industry standard temperature sensor available in a TO-92 package. Unlike more expensive bi-metallic thermocouples, its output is immune to electrostatic and electromagnetic fields, which will undoubtedly be present in the system.

A 4-pin header on the board, J2, provides the necessary 15 volts and ground to power the LM35. The LM35 feeds back a voltage proportional to temperature, which is scaled, buffered and available on pin 11 of J1.

The scaling of the signal on pin 11 of J1 is 1V/12°C, where 0 volts is 0°C. The over temperature threshold is set on the GDB at 98 ±2°C, which corresponds to 8.17 volts at pin 11. The threshold can be adjusted for a specific application.

Protection Features

The APS GDB is equipped with several protection features that will prevent catastrophic system failures. In the case of one of the faults discussed below, all gate drive signals are latched off (customer provided control signals are inhibited from reaching the gates) and the LED associated with the fault will light. The GDB will remain in a latched off state until all customer provided control

signals are held low for at least 8μs. When both control signals are held low for a minimum of 8μs, the latched fault will be reset. If the cause of the fault condition is removed, the control signals will be applied to the gates and the LED will be extinguished.

Reset Function

This 8□s reset feature is the reason that user generated dead time is neither required nor desired. If dead time of 8□s is supplied with the control signals, the unit will not properly latch off on fault event and will continue to fire during fault conditions. If an over current fault exists, the GDB will protect itself and the IGBTs on a pulse-by-pulse basis. However, the IGBTs may not be able to turn on into this condition indefinitely. Therefore, the control logic should heed the warning of the fault signals and inhibit the control signals when a fault condition is indicated.

Over Current Protection

The first form of over current protection compares the feedback from each Hall effect sensor to a predetermined threshold. When the threshold is exceeded, all gate drive signals are latched off within 2μs. They remain latched off until the fault condition is removed and all customer provided control signals are held low for at least 8μs.

The over current threshold should be set such that the voltage overshoot, due to the DC link inductance (see System Considerations), resulting at turn off does not reach destructive levels for the IGBTs being used.

The second form of over current protection on the three-phase GDB is used only with Powerex F-series IGBTs. When an over current condition is detected, the gate-emitter voltage is reduced to limit short circuit current. The APS GDB senses this condition and performs a soft turn-off of the IGBT conducting the excessive current. This form of over current is typically a shoot through with no load impedance to limit its magnitude. Therefore, a soft turn off is necessary to limit the voltage overshoot at turn off to a safe level. Upon detection of this condition the soft turn off is performed, all gate drive signals are latched off, and the associated phase's LED is illuminated. The gate signals remain latched off until the fault condition is removed and all customer provided control signals are held low for at least 8μs. An over current or short circuit fault output signal is annunciated for each phase leg on J1-pins 3, 6 and 9, see page 10 for additional information.

Over Voltage Protection

The over voltage protection senses the DC link input and compares it to a predetermined threshold, 910 volts for 1200 volt devices and 450 volts for 600 volt devices. When the threshold is exceeded for more than 1ms, the gate pulses are latched off 2μs later, and the over voltage LED is illuminated. The gate signals remain latched off until the fault condition is removed and all customer provided control signals are held low for at least 8μs. An over voltage fault output signal is annunciated on J1 pin 11, see page 10 for more information.

Over Temperature Protection

The over temperature protection uses the temperature sense input and compares it to a predetermined threshold, 98 ± 2°C. When the threshold is exceeded for 1ms, the gate pulses are latched off 2μs later and the over temperature LED is illuminated. The gate signals remain latched off until the temperature sense input goes below 98°C and all customer provided control signals are held low for at least 8μs. An over temperature fault output signal is annunciated on J1 pin 11, see page 10 for more information.

Under Voltage Lock Out (UVLO)

The UVLO protection monitors the 15-volt logic supply, latches off the gate pulses and illuminates the UVLO LED if the 15-volt supply dips below 12 volts.

There is also an UVLO on each gate drive chip. When the power supply for a gate drive chip droops to a value that precludes the IGBT from being driven into saturation, the gate pulses are latched off and the associated phase's over current LED is illuminated. The gate signals remain latched off until the fault condition is removed and all customer provided control signals are held low for at least 8□s. A UVLO fault output signal is annunciated on J1 pin 11, see page 10 for more information.

Connecting the APS GDB to a Three Phase System

In order for the APS GDB to interface with a power stage, several connections need to be addressed:

Ribbon Cable connector J1 – A 26 pin ribbon cable connector (3M part #3399-7600 with strain relief part #3448-3026 or an equivalent) is required to interface the GDB with the customer provided controls. Pin assignments are detailed in **Table 1.** If the control logic already exists without a 26-pin header, terminal block to 26-pin header adapters are available.

Gate Leads – The power stage should be packaged so the gate leads are as short as possible. The gate leads should be a twisted pair of 22 AWG wires (approximately 2-3 turns per inch) no more than two feet long, preferably 4-6 inches long. There are through holes located next to the solder pads for each gate and emitter connection on the GDB. These provide a low cost, reliable strain relief by feeding the wire through the blank hole and then soldering the wire to the pad next to it.

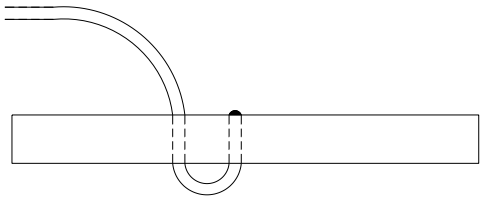


Figure 3: Strain relief connection.

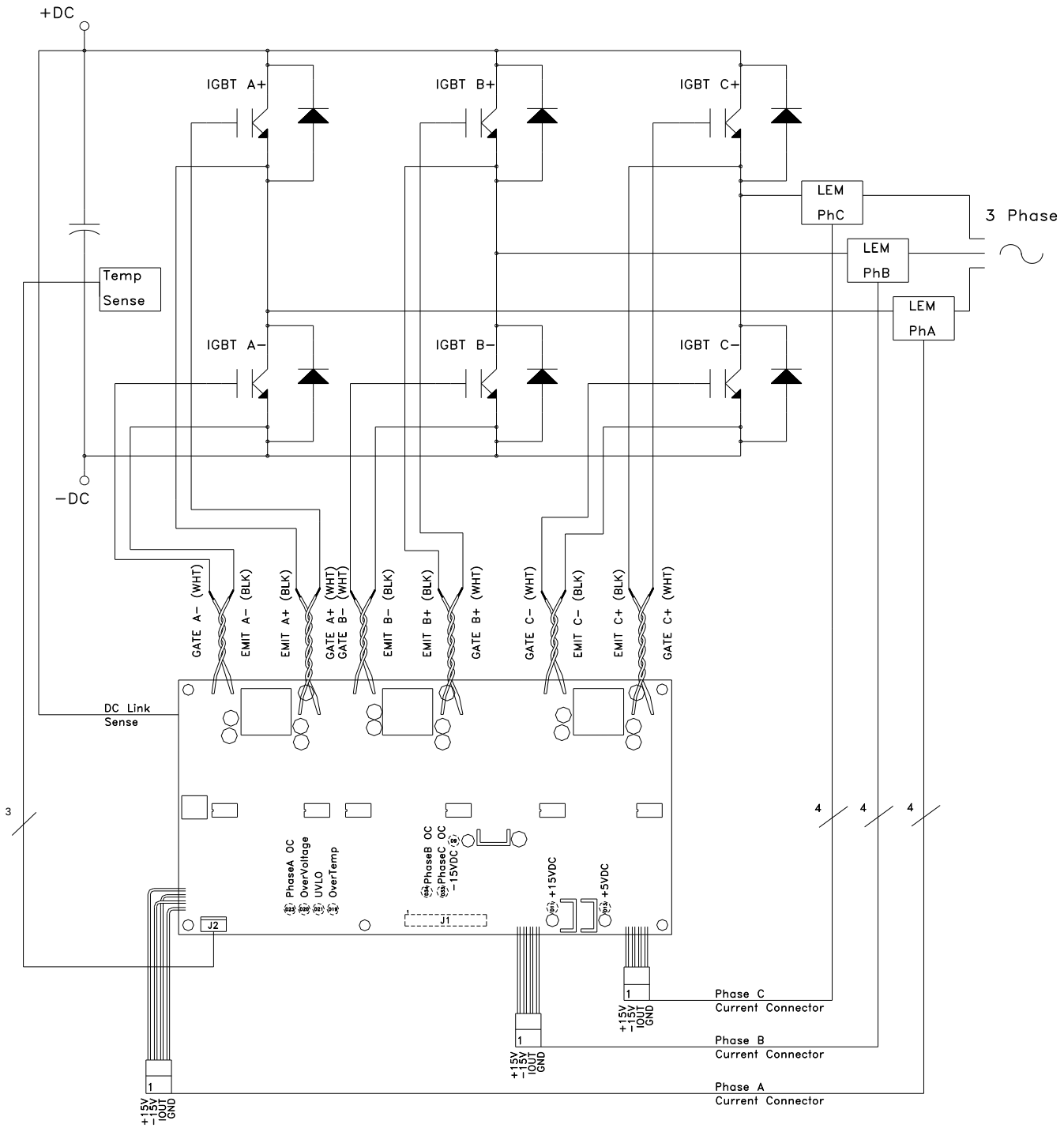
Standard gate lead lengths supplied are 3.5" long. Longer or shorter leads are available upon request. Please see the form at the end of this Datasheet/Application Note for additional information.

The interface with the IGBTs will be either a standard .110 fast-on or a ring terminal; depending upon the IGBT module being used.

DC Link Connection – The DC link monitoring and over voltage protection are made possible by the DC link connection, which should be a single 22 AWG wire with a ring terminal on the end to connect to the positive of the DC link. This wire's interface with the GDB uses the same strain relief technique detailed in the gate lead section above.

Current Sense Connection – The GDB provides a four-wire connection for current sensing of each of the three phases. The connections are clearly labeled on the GDB and are the required connections to interface with the HAS or HAC series of Hall Effect Sensors from LEM, or equivalent (**Note:** The sequence of the GDB connections for phase A is not the same as the sequence for phases B and C). To make the connections to the GDB, 22 AWG is recommended employing the strain relief technique depicted in **Figure 3**. However, since the four connections for each LEM have .100" spacing, many connectors may be inserted in the board. The LEM interface uses a four-pin Molex connector part # 5045-04A. The system designer may use the Molex mate or an insulation displacement connector, such as the AMP part # 640440-4, will work as well.

Temperature Sense – A 4-pin header, J2, is provided on the GDB to interface with the three terminal temperature sense. A 4-pin header is used in lieu of a three-pin header to provide additional structural integrity and the same connector, AMP P/N 640440-4, may be used. Pin assignments are provided in **Table 2.**


+DC
IGBT A+
IGBT B+
IGBT C+
LEM PhC
3 Phase
LEM PhB
LEM PhA
Temp Sense
IGBT A−
IGBT B−
IGBT C−
−DC
GATE A− (WHT)
EMIT A− (BLK)
EMIT A+ (BLK)
GATE A+ (WHT)
GATE B− (WHT)
EMIT B− (BLK)
EMIT B+ (BLK)
GATE B+ (WHT)
GATE C− (WHT)
EMIT C− (BLK)
EMIT C+ (BLK)
GATE C+ (WHT)
DC Link Sense
3
4
4
4
PhaseA OC
OverVoltage
UVLO
OverTemp
PhaseB OC
PhaseC OC
−15VDC
+15VDC
+5VDC
J1
J2
+15V
−15V
IOUT
GND
Phase C Current Connector
Phase B Current Connector
Phase A Current Connector

System Considerations

There are many issues to consider when packaging a power stage including capacitor selection and configuration, routing of high current connections, heat sink size, and air or liquid cooling. These issues should be considered at the design stage and if not adequately addressed, a reliable power stage may never be realized.

Capacitors should be selected with ripple current capabilities sufficient for the particular application. For safety purposes, permanent bleeder resistors should be installed across the capacitors to ensure they are discharged when the power stage is turned off. The connection from the capacitors to the IGBTs should contain as low inductance as possible. Making this connection with a laminated bus is the most effective technique for minimizing bus inductance. A laminated bus uses flat sheet conductors separated by a thin insulator to force opposing currents to cancel magnetic fields thereby minimizing the inductance of the current path.

Low inductance will minimize voltage overshoots at turn off and minimize, if not eliminate the need for snubber capacitors. The voltage overshoot should be measured under controlled pulsed conditions at the over current threshold to be sure that IGBTs will not be destroyed due to over voltages.

Stray capacitance from the electrical connections within the IGBT to its baseplate exist. The high dV/dts inherent in IGBT based power stages will conduct current through this stray capacitance that may cause the heatsinks containing the IGBTs to float to **dangerously** high potentials. For this reason as well as to minimize noise coupling into the GDB, it is recommended that heatsinks be grounded.

Heatsinks should be sized to dissipate the heat generated by the operation of the IGBTs. The total power loss (conduction losses and switching losses) of an IGBT power stage can be closely approximated using calculations based on IGBT and system parameters (APS applications engineers are available to assist with these calculations in certain situations). However, the calculated estimates should always be verified with empirical testing. Consult APS for heatsink and bus bar recommendations.

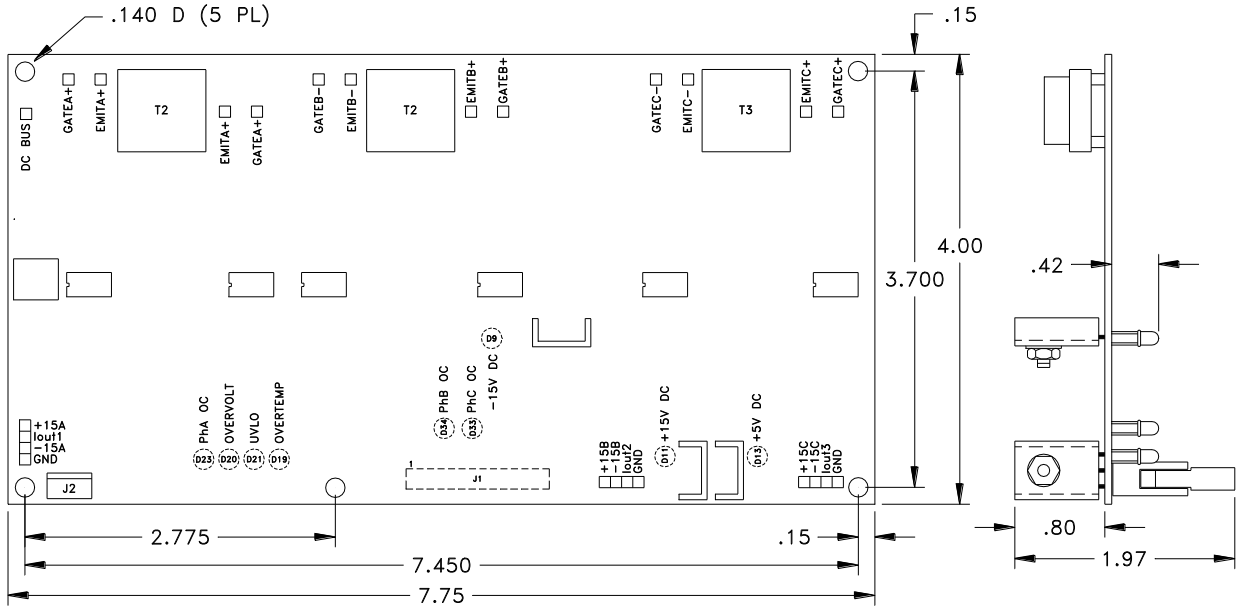


Figure 10: Mechanical drawing.

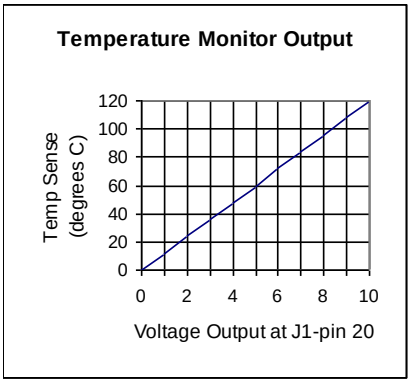


Figure 5: Feedback scaling can be modified, consult APS.

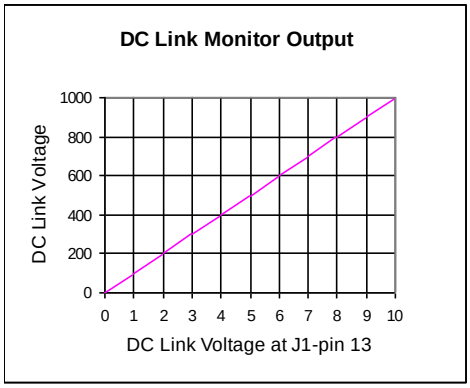


Figure 6: Feedback scaling can be modified, consult APS.

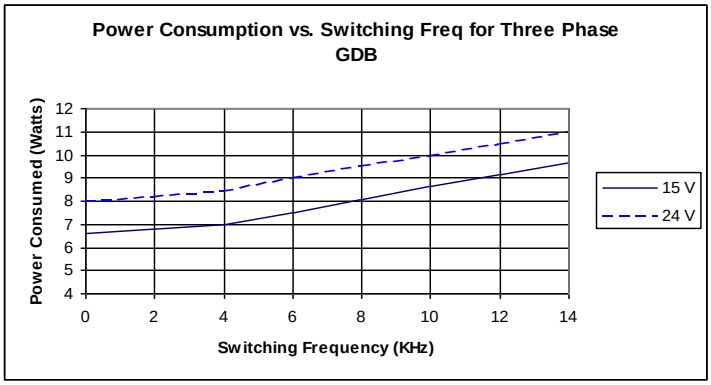


Figure 7: GDB driving three dual IGBTs with gate charge of 1100µC.

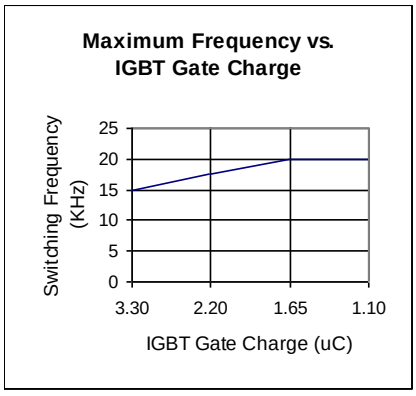


Figure 8: GDB driving three dual IGBTs with indicated Gate charge. Modifications can be made to operate at higher frequencies.

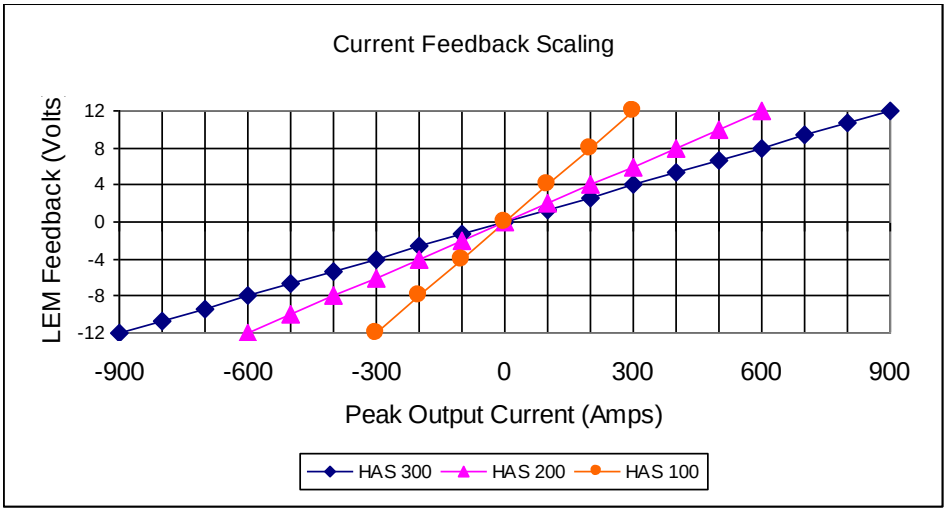


Figure 9 Standard current scaling, can be modified consult APS.

J1[5]

Pin	Signal Name	Description
1	Shield	Connected to circuit ground
2	PWM A-	0-15 V signal controls the duty cycle of A- IGBT
3	Phase A Error[1]	Open collector output, external pull-up resistor required; LOW = No Error; Floating = Phase A overcurrent or short circuit
4	PWM A+	0-15 V signal controls the duty cycle of A+ IGBT
5	PWM B-	0-15 V signal controls the duty cycle of B- IGBT
6	Phase B Error[1]	Open collector output, external pull-up resistor required; LOW = No Error; Floating = Phase B overcurrent or short circuit
7	PWM B+	0-15 V signal controls the duty cycle of B+ IGBT
8	PWM C-	0-15 V signal controls the duty cycle of C- IGBT
9	Phase C Error[1]	Open collector output, external pull-up resistor required; LOW = No Error; Floating = Phase C overcurrent or short circuit
10	PWM C+	0-15 V signal controlling the duty cycle of C+ IGBT
11	Overtemp, Over Voltage, or UVLO Error[1,4]	Open collector output, external pull-up resistor required; LOW = No Error; Floating = Overtemp, DC link over voltage ,or UVLO
12	Not Connected	
13	DC Link Voltage	Scaled analog representation of DC link voltage
14	24 VDC input power[2]	20 – 30 VDC input voltage range, unregulated
15	24 VDC input power[2]	20 – 30 VDC input voltage range, unregulated
16	15 VDC input power[2]	14.4 – 15.6 VDC input voltage range, regulated
17	15 VDC input power[2]	14.4 – 15.6 VDC input voltage range, regulated
18	GND	Ground reference for 15 or 24 VDC inputs
19	GND	Ground reference for 15 or 24 VDC inputs
20	Heatsink Temperature	Analog voltage representation of heatsink temperature; 0V represents 0°C, 10V represents 120°C
21	GND[3]	Tied to pins 18 and 19
22	Iout Phase A	Analog voltage representation of phase A output current; current feedback scaling is dependent on customer selected transducer and gain of signal conditioning circuitry on GDB
23	GND[3]	Tied to pins 18 and 19
24	Iout Phase B	Analog voltage representation of phase B output current; current feedback scaling is dependent on customer selected transducer and gain of signal conditioning circuitry on GDB
25	GND[3]	Tied to pins 18 and 19
26	Iout Phase C	Analog voltage representation of phase C output current; current feedback scaling is dependent on customer selected transducer and gain of signal conditioning circuitry on GDB

Notes:

1. Open collector outputs may be pulled up to 30 V max and sink 50mA continuous.
2. Do not connect a 15 VDC and 24 VDC source to the unit at the same time, use one or the other.
3. GND signals to be used for analog feedback signals, i.e. twisted pair with Iout Phase A.
4. The error signal on pin 11 is the ORed output of the Over voltage, Overtemp, and UVLO fault signals. An LED will illuminate to differentiate specific fault type.
5. Mating connector is P/N: 3M 3399-7600 and strain relief is P/N: 3448-3026.

J2

1	+15 Volts	15 volts from GDB
2	Temp Sense Output	Analog Temp Sense output
3	GND	GND reference for +15 Volts, tied to ground of 15 or 24 volt supply
4	NC	No connection

Current Feedback Connectors

1	+15 Volts	15 volts from GDB
2	-15 Volts	-15 volts from GDB
3	Iout (A, B, & C)	Voltage proportional to output current
4	GND	GND of GDB control logic

There are three "headers" available on the board to interface with three separate Hall effect sensors (LEMs). Headers are not installed on the board to allow for the strain relief hook-up detailed in Figure 3. However, the pads are separated by standard .100 spacing to allow for the installation of headers with .100 spacing. **Note:** The wiring for the B and C connectors is 1 to 1, i.e. pin 1 on the GDB goes to pin 1 on the LEM, pin 2 goes to pin 2, pin 3 to pin 3, and pin 4 to pin 4. Pin 2 and pin 3 are reversed at the GDB for the phase A connector. This is illustrated in the diagrams in Figures 4 and 10.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to GND of GDB Power Supply)

Parameter	Value	Units
Unregulated 24 VDC Power Supply	30	V
Regulated 15 VDC Power Supply	15.5	V
PWM Input High	20	V
PWM Input Low	-5	V
Fault Output Supply Voltage	30	V
Fault Output Current (sink)	50	mA
DC Link Voltage Input	1000	V
Switching Frequency	See Figure Below	Hz

ELECTRICAL CHARACTERISTICS

Characteristic	Min	Typ	Max	Unit
Unregulated 24 VDC Power Supply	20	24	30	V
Regulated 15 VDC Power Supply	14.5	15	15.5	V
PWM Input ON Threshold*	12	15		V
PWM Input OFF Threshold		0	2	V
Gate Drive Output Voltage High	13	15	18	V
Gate Drive Output Voltage Low	-6	-5	-3.5	V
OverTemp Threshold	98	100	102	°C
OverVoltage Threshold	900	910	920	V
Temp Sense Feedback	See Figure Below			V
DC Link Voltage Feedback	See Figure Below			V
GDB Power Consumption from 24 or 15 VDC	See Figure Below			Watts

NOTE: The AP-1491 can be modified to accept TTL level PWM control signals. See Fax form at the end of this Datasheet/Application Note.

APS Fax Request Form

Fax # (516) 935-2603

The BAP1491 Gate Drive Board has many parameters that can be tailored to your application. Please provide the information below to modify your gate drive board and FAX it an all other questions or comments to the number above.

Name: _____ Company: _____

Phone #: _____ Fax #: _____

E-mail Address: _____

Application description: _____

_____

_____

APS GDB Configuration: ❑ Three Phase ❑ Full Bridge ❑ Half Bridge

IGBT blocking voltage: ❑ 1200 Volts ❑ 600 Volts ❑ Other_____

Over Voltage Set point: ❑ 900 Volts ❑ 450 Volts ❑ Other_____

Dead Time Request if different than 2µs: ____µs Over Current Threshold (A): ____A

Requested gate resistor if different from 4.3 Ohms: _____Ω

Over Temperature threshold if different from 98°C: _____°C

Gate Lead Termination: ❑ .110 Fast-on ❑ Ring Terminal ❑ Other: _____

Modify the AP-1491 to accept TTL PWM control signals: ❑

Quantity of Boards: _____ per: ❑ year ❑ month ❑ total ❑ Quote only

Comments: